CLAIMS

1. A method for re-targeting a design, said method comprising the steps of:

receiving a first low-level design representation targeting a first integrated circuit;

transforming said first low-level design representation into a synthesizable; editable, and simulatable high-level design representation; and

processing said high-level design representation to generate a second low-level design representation targeting a second integrated circuit.

2. The method of claim 1 wherein one of said first and said second integrated circuits is complex programmable logic device.

3. The method of claim 1 wherein one of said first and said second integrated circuits is field programmable gate array.

4. The method of claim 1 wherein one of said first and said second integrated circuits is gate array.

5. The method of claim 1 wherein one of said first and said second integrated circuits is ASIC.

6. The method of claim 1 wherein said high-level design representation comprises VHDL code.

7. The method of claim 1 wherein said high-level design representation comprises ABEL code.

8. The method of claim 1 wherein said high-level design representation comprises Verilog code.

9. The method of claim 1 wherein said low-level design representation comprises boolean equations.

10. The method of claim 1 wherein said transforming steps comprises the steps of:

parsing said first low-level design representation;

identifying equations in said first low-level design representation that give rise to synthesizable and simulatable objects; and

writing said high-level design representation that contains said synthesizable and simulatable objects.

11. The method of claim 10 wherein said objects include flip flops.

12. The method of claim 10 wherein said objects include input, output and inout.

13. The method of claim 10 wherein said objects include tristate and open drain outputs.

14. The method of claim 10 wherein one of said first and said second integrated circuits is complex programmable logic device.

15. The method of claim 10 wherein one of said first and said second integrated circuits is field programmable gate array.

16. The method of claim 10 wherein one of said first and said second integrated circuits is gate array.

17. The method of claim 10 wherein one of said first and said second integrated circuits is ASIC.

18. The method of claim 10 wherein said high-level design representation comprises VHDL code.

19. The method of claim 10 wherein said high-level design representation comprises ABEL code.

20. The method of claim 10 wherein said high-level design representation comprises Verilog code.

21. The method of claim 10 wherein said low-level design representation comprises boolean equations.